

# PS2 Keyboard

## About the guide

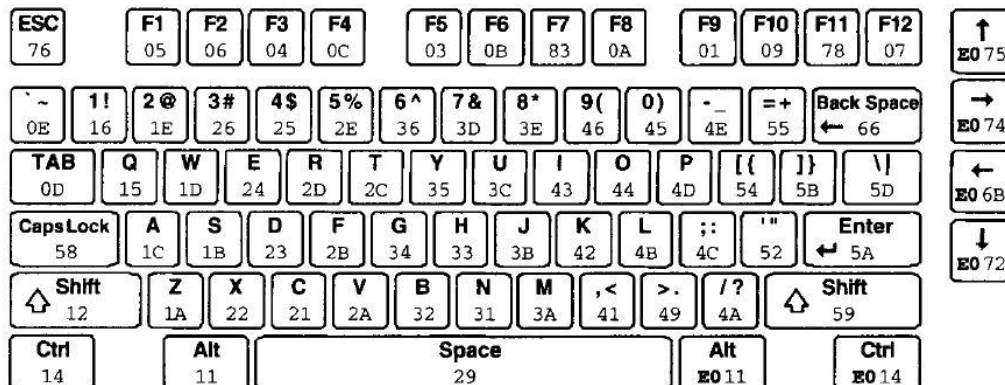
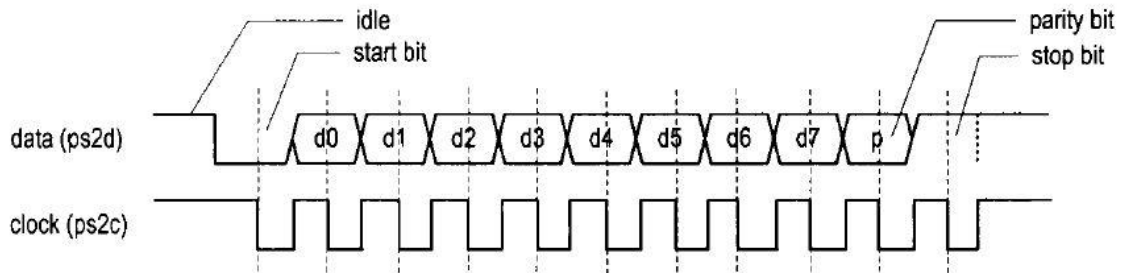
Aim of this guide is to make you familiar with ps2 protocol and building a keyboard module in verilog.

## Protocol

Protocol is synchronous using two pins one clock pin another data pin. Data is supposed to be sampled at falling edge of clock pin. Data is sent in packet of 11 bits. First start bit "0", next 8 bits data, next parity then ending bit "1".

Eight data bits are distinct for each key.

When you press a key keyboard continuously send data bits corresponding to that key continuously until it is pressed then keyboard sends ending byte 'f0'.



For example if 'a' is pressed then 1c will be transmitted multiple times and bytes received are 1c,1c,1c.....1c,f0.If shift then a is pressed then bytes transmitted will be 12,12...12,1c,....1c,f0,12,.....,12,f0.

Verilog Code:-

```
module keyboard(
input wire clk,          // Clock pin form keyboard
input wire data,        //Data pin form keyboard
output reg [7:0] led    //Printing input data to led
);
reg [7:0] data_curr;
reg [7:0] data_pre;
reg [3:0] b;
reg flag;

initial
begin
b<=4'h1;
flag<=1'b0;
data_curr<=8'hf0;
data_pre<=8'hf0;
led<=8'hf0;
end

always @(negedge clk) //Activating at negative edge of clock from keyboard
begin

case(b)
1:; //first bit
2:data_curr[0]<=data;
3:data_curr[1]<=data;
4:data_curr[2]<=data;
5:data_curr[3]<=data;
6:data_curr[4]<=data;
7:data_curr[5]<=data;
8:data_curr[6]<=data;
9:data_curr[7]<=data;
10:flag<=1'b1; //Parity bit
11:flag<=1'b0; //Ending bit

endcase

if(b<=10)
b<=b+1;

else if(b==11)
b<=1;

end

always@(posedge flag) // Printing data obtained to led
begin

if(data_curr==8'hf0)
led<=data_pre;

else
data_pre<=data_curr;
end endmodule
```

Tips:-

- 1) Add "NET "[Keyboard clock pin]" CLOCK\_DEDICATED\_ROUTE = FALSE;" to your constraint file.
- 2) Pull up both clock and data pins in your constraint file.
- 3) Scan code send by keyboard are not ascii code you must manipulate it according to your use.