

Getting Started

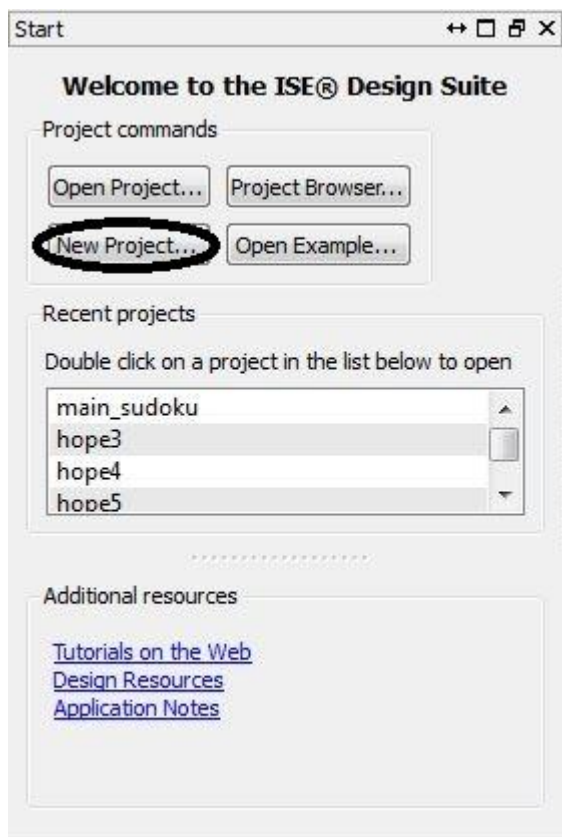
Aim of this document is to make you familiar with software interface of Xilinx ISE by loading a pre-build programme to our FPGA .This guide is for Xilinx ISE 14.1 but other versions are also identical.

Downloading Software:-

You may either download Evaluation Version(one month) or purchase a new licence from [here](#). Install this software in your pc.

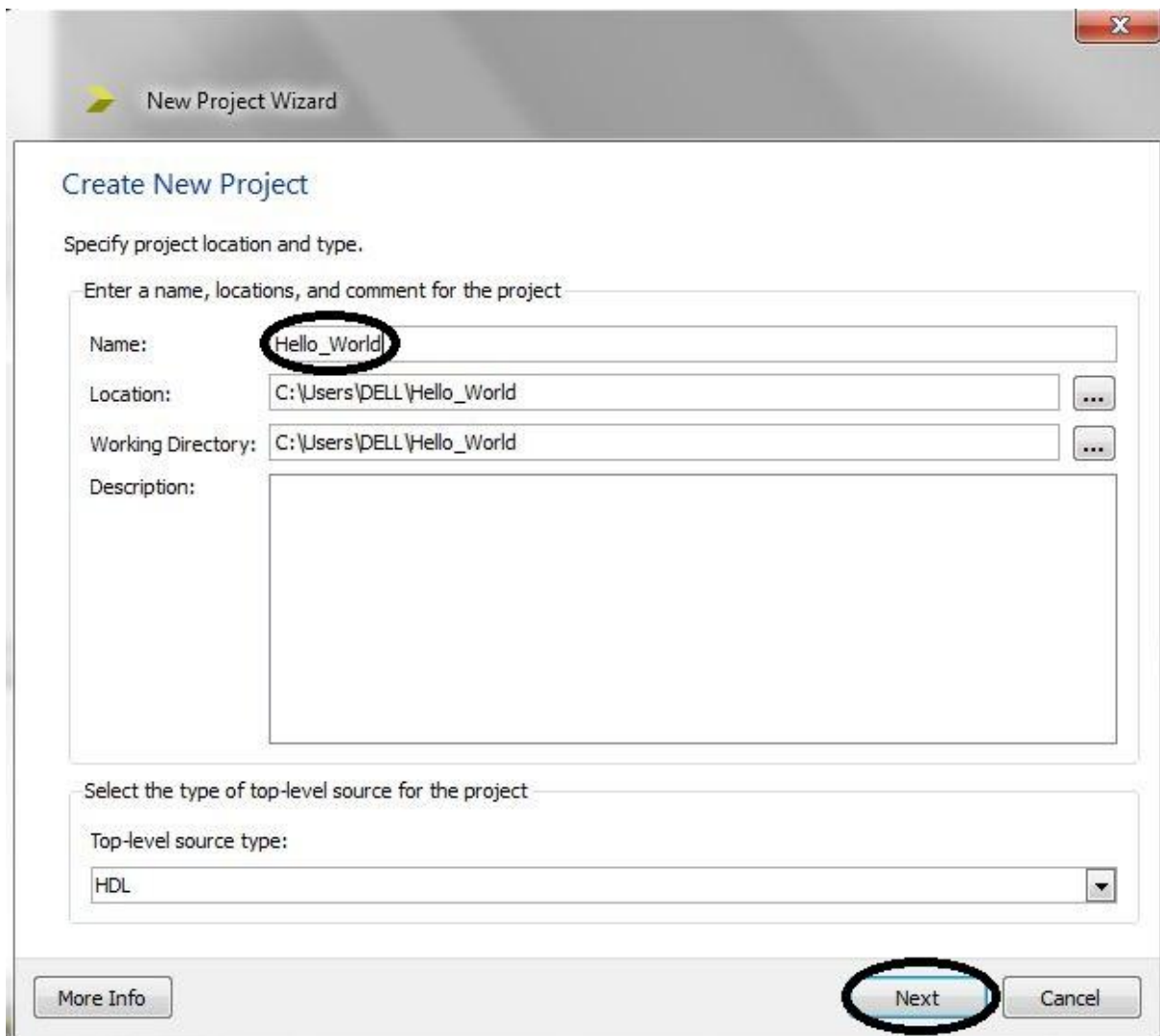
Creating new project:-

1.



Open Xilinx ISE->Click on new project.

2.



Give your project a name and click next.

3. Fill the required fields :-

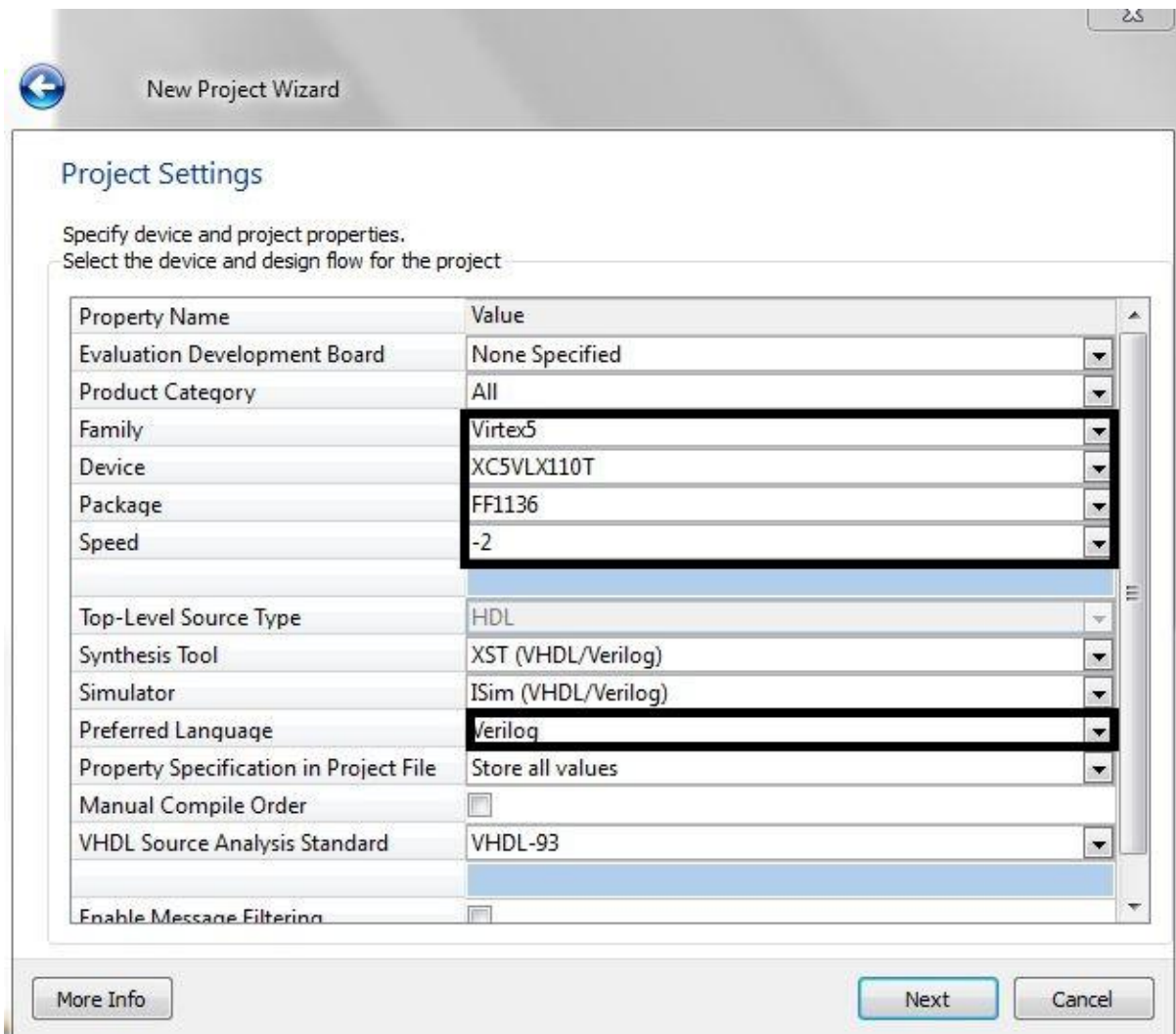
For board in club:-

Family->Virtex 5

Device->XC5VLX110T

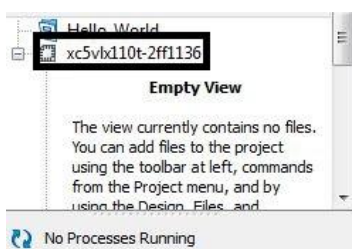
Package->ff1136

Speed -> -2.

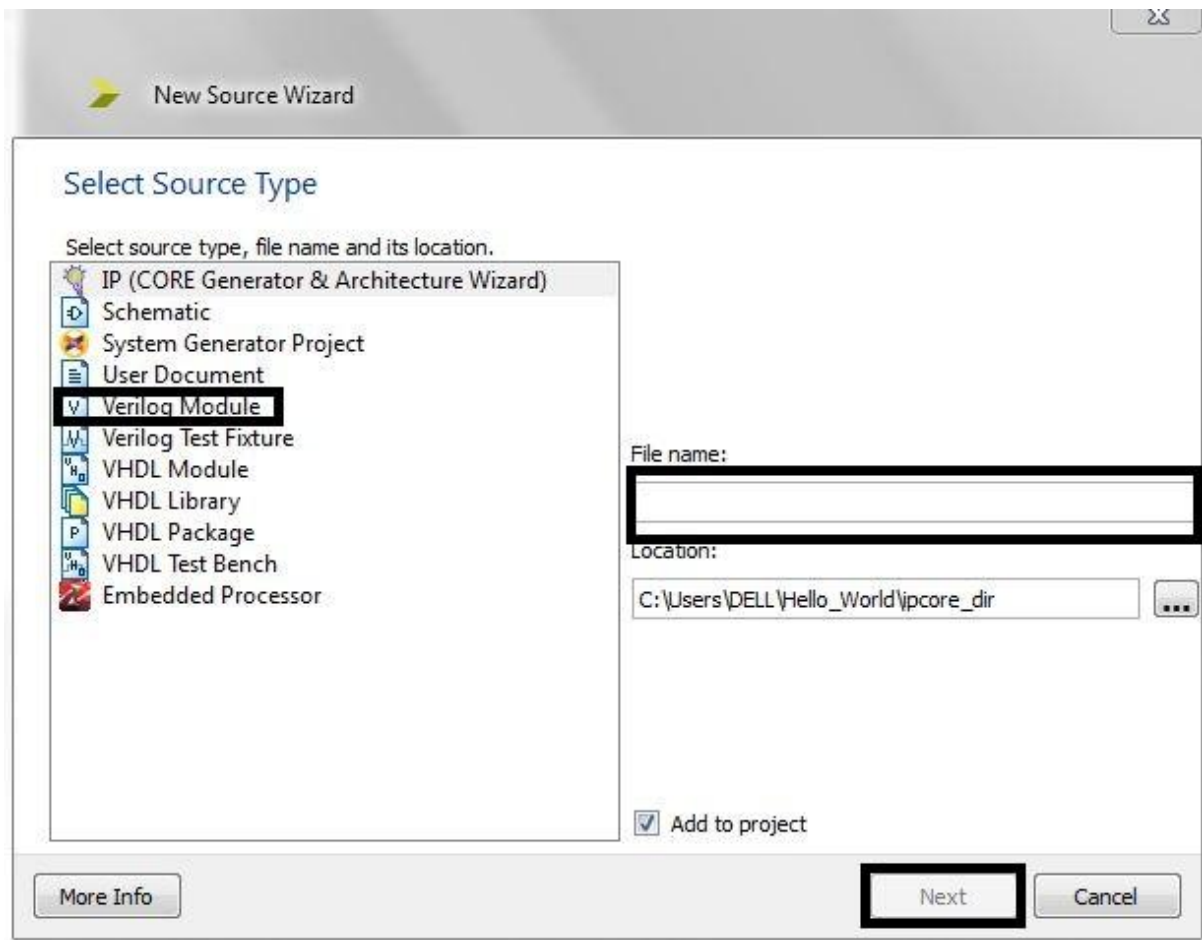


After this click Finish.

Making our first project:-



Right click on this option & select new source.



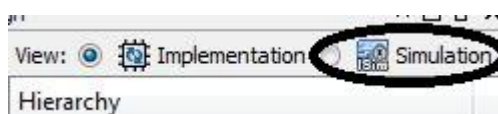
Click on Verilog Module->Give file a name->Then click next->again click next then finish.

Similarly you can add .ucf file used for hardware communication.

Let us take a example close this porject and download <http://students.iitk.ac.in/eclub/database.php>->Digital Logic Design Using Verilog and FPGA Devices 2010->LCD_DRIVER->LcdDriver Xilinx ISE Project file open this file from open project or double click on it.

Now simulate this file:-

1.



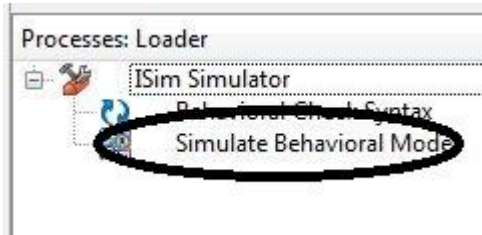
Click on simulate button.

2.

Click on Loader.v



Double click on Simulate Behavioral Model



3.

Right click on CLK->Force Clock->Leading edge [1]->Falling edge[0]->Time period as you wish minimum 2ps.

Object Name	Value
CLK	z
LCDDATA[7:4]	XXXXX
LCD_RS	x
LCD_RW	x
LCD_E	x
FREQGEN[25:0]	0000
lcd_stb	x
lcd_code[5:0]	XXXXX
lcd_stuff[6:0]	XXXXX

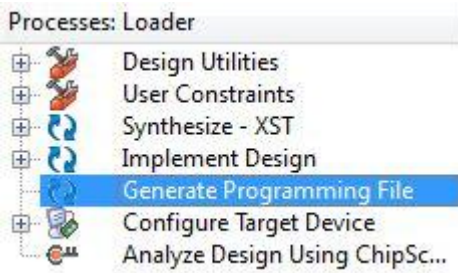
4.

Click on play and pause simulation after sufficient time.



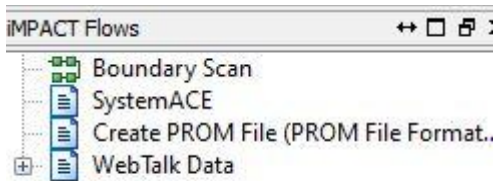
Now implementing our code to our fpga:-

1. Go back to ISE->Implementation



Generate Programming File.
Then Configure Target Device.

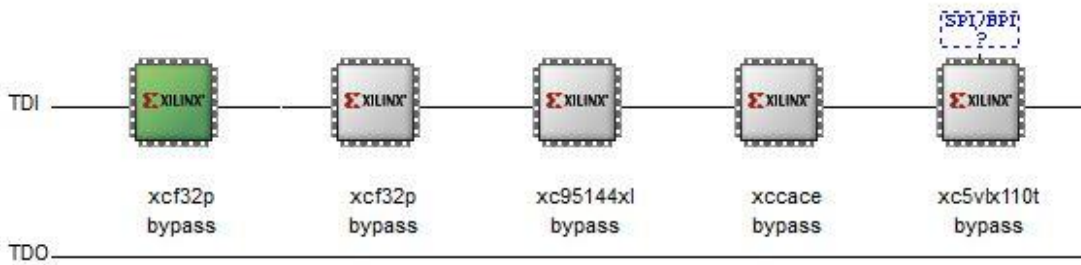
2.



Boundary Scan->Right Click on centre ->Initialize Chain

3.

You should get this if all thing is correct



Some tips->

- 1) Don't forget to power on FPGA.
- 2) Connect jtag cable correctly
- 3) Check if Programming cable is not faulty. Many cables in club are faulty.

Double click on xc5vlx110t icon(5th from starting) load loader.bit.

Click no to "Attach spi or BPI PROM pop up".

Right click on same icon then "Program" .

Take this document just as a test drive.