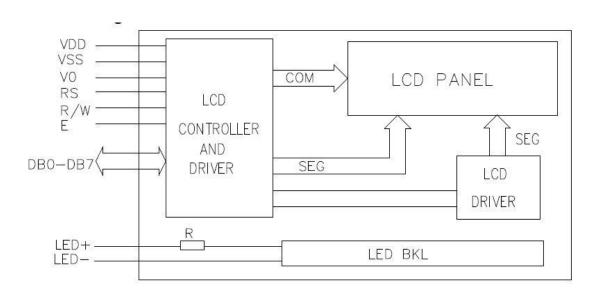
ALPHANUMERIC LCD

This document will tell you working of 16x2 alphanumeric lcd.

Basic Pin & Description:

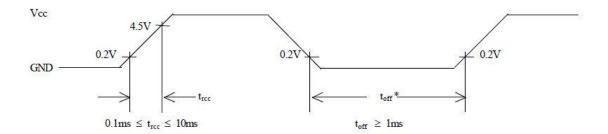
Pin no.	Symbol	External connection	Function			
1	Vss		Signal ground for LCM			
2	V _{DD}	Power supply	Power supply for logic for LCM			
3	Vo		Contrast adjust			
4	RS	MPU	Register select signal			
5	R/W	MPU	Read/write select signal			
6	E	MPU	Operation (data read/write) enable signal			
7~10	DB0~DB3	MPU	Four low order bi-directional three-state data bus lines. Used for data transfer between the MPU and the LCM. These four are not used during 4-bit operation.			
11~14	DB4~DB7	MPU	Four high order bi-directional three-state data bus lines Used for data transfer between the MPU			
15	LED+	LED BKL power	Power supply for BKL			
16	LED-	supply	Power supply for BKL			



Initialization Protocol:

1. Initialization using the Internal Reset Circuit

The display can be initialized using the internal reset circuit if the Internal Power Supply Reset timing below is met.



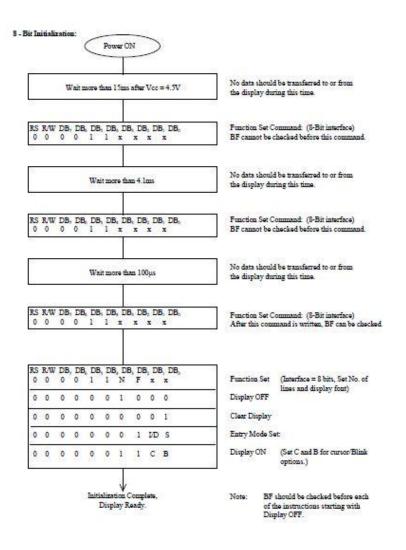
Note: toff represents the time of power off condition for a momentary power supply dip or when cycling power off then on.

If the internal power supply reset timing cannot be met, the display will not operate normally. In this case, the display can be initialized through software.

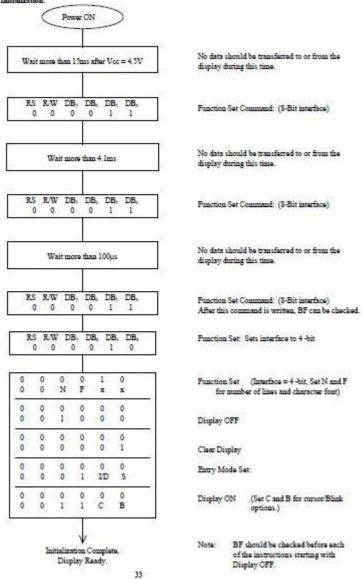
Note: Variable power supply may affect timing hence initialization of lcd in that case software initialization is preferred.

2. Software Initialization

Although software initialization is not mandatory, it is recommended that this procedure always be performed







Instruction Set:

Instruction	Code RS R/W DB. DB. DB. DB. DB. DB. DB. DB.								DB.	Description	Execution time (max.) when fcp or fosc is 250 kHz	
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DD RAM address 0 in address counter.	15.2ms
Return Home	0	0	0	0	0	0	0	0	1	х	Sets DD RAM address 0 in address counter. Also returns shifted display to original position. DD RAM contents remain unchanged.	15.2ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies shift or display. These operations are performed during data write and read.	40µs
Display ON/OFF Control	0	0	0	0	0	0	1	D	С	В	Sets ON/OFF of entire display (D), cursor ON/OFF (C), and blink of cursor position character (B).	40µs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	x	x	Moves cursor and shifts display without changing DD RAM contents.	40μs
Function Set	0	0	0	0	1	DL	N	F	x	x	Sets interface data length (DL), number of display lines (N) and character font (F).	40µs
Set CG RAM Address	0	0	0 1 ACG								Sets CG RAM address. CG RAM data is sent and received after this setting.	40µs
Set DD RAM Address	0	0	1 ADD								Sets DD RAM address. DD RAM data is sent and received after this setting.	40µs
Read Busy Flag & Address	0	1	BF AC								Reads busy flag (BF) indicating internal operation is being performed and reads address counter contents.	40μs
Write Data to CG or DD RAM	1	0	Write Data								Writes data into DD RAM or CG RAM.	40µs
Read Data from CG or DD RAM	1	1	Read Data								Reads data from DD RAM or CG RAM.	40µs
	I/D=1: Increment I/D=0: Decrement S=1: Accompanies display shift S/C=1: Display shift S/C=0: Cursor move R/L=1: Shift to the right									DD RAM: Display Data RAM CG RAM: Character Generator RAM ACG : CG RAM address ADD : DD RAM address. Corresponds to cursor address. AC : Address counter used for both	Execution time change: when frequency changes: Example: When fcp or fosc is 270kHz:	

Scan Code:

Table 5.3 Standard Character Fout Table 0000 0010 0011 0100 0110 0111 1010 1011 1100 1101 1110 1111 Low order bi CG RAM a 0 œ P F> X X X X0000 7 P Q 43 4 4 ēi !2 (2) X X X X0001 2 4 ŋ В R × Θ Ю r β X X X X0010 # Ż 5 S 7 芒 C 8 w X X X X0011 d \$ ŧ. D ψ Ι H Ω X X X X0100 % 7 7 E U e IJ ø u X X X X0101 8: = 6 ĴŢ ρ Ų 7 X X X X0110 G W ŧ 9 9 6 7 77 ΊŢ X X X X0111 (8) Xh 7 求 IJ (8 × $\bar{\times}$ 1 X X X X1000 1 y t ĮĮ, X X X X1001 şķ 1/ Z Ü Œ XXXXI010 (3) E { K k -ÿ 77 ኧ XXXXIOII 77 4 iΞ 7 Ť X X X X 1100 (5)

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Note: Software initialisation is always preferred.