AUBTM-20

Bluetooth V2.0 Class 2 module

Product datasheet

General Description

AUBTM-20 is Bluetooth Core V2.0 compliant module with SPP. The module is designed to be embedded in a host system which requires cable replacement function. Typically the module could interface with a host through the UART port.
The module could be used in many different application, e.g.:
• Hand held terminals
• Industrial devices
• Point-of-Sale systems
• PCs
• Personal Digital Assistants (PDAs)
• Computer Accessories
• Access Points
• Automotive Diagnostics Units
This module could both act a SPP master and a SPP slave. When in master mode, the module could search for all the working SPP slave devices around and the host could select which to connect. When it is in slave mode, it will listen for connection request from another SPP master device.

Key Specification

- Bluetooth core V2.0 compliant
- SPP support
- Support UART,USB,PCM,I2C interface to host system

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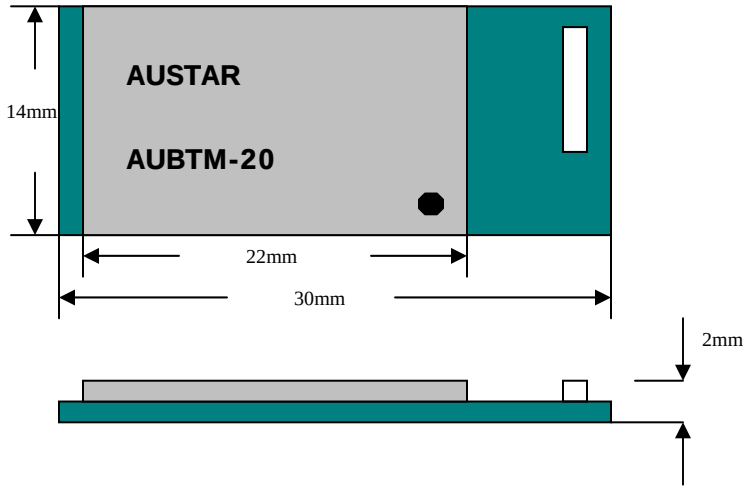
1. Physical Dimension:



2. Block Diagram

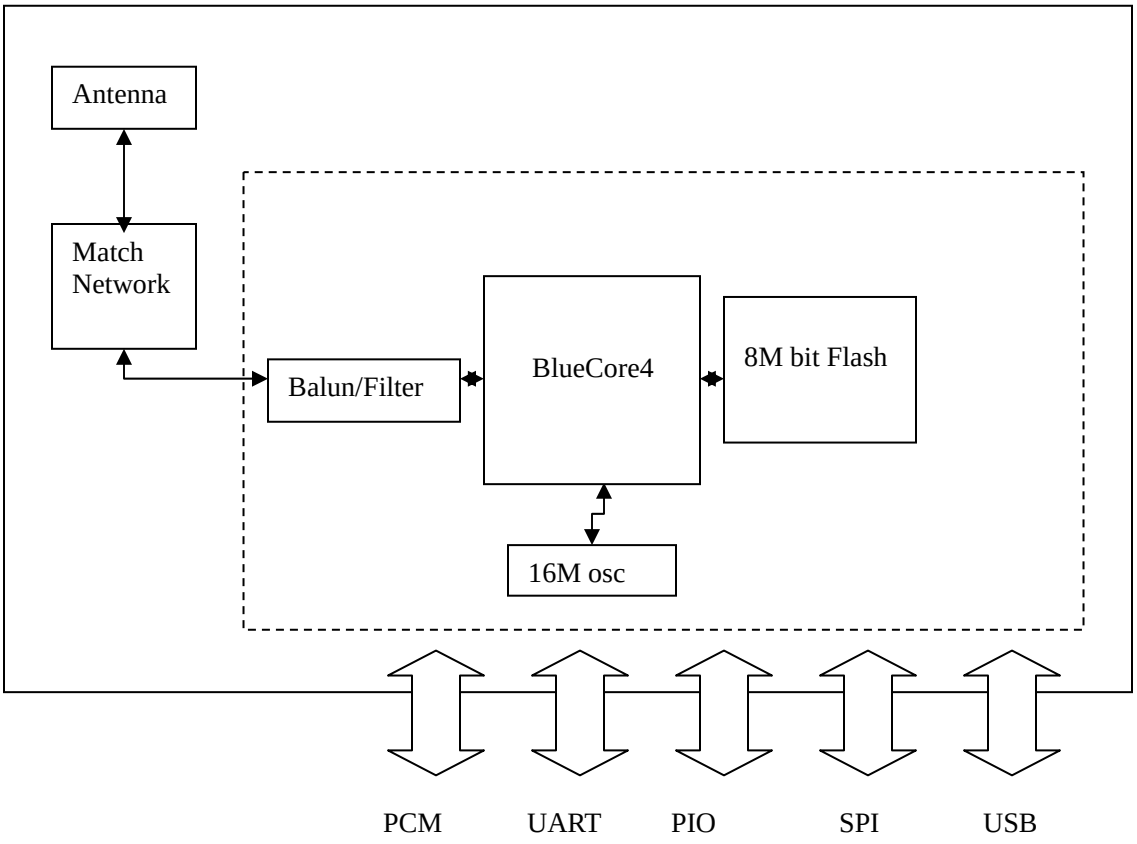


Fig.1 Block Diagram

3. Foot print

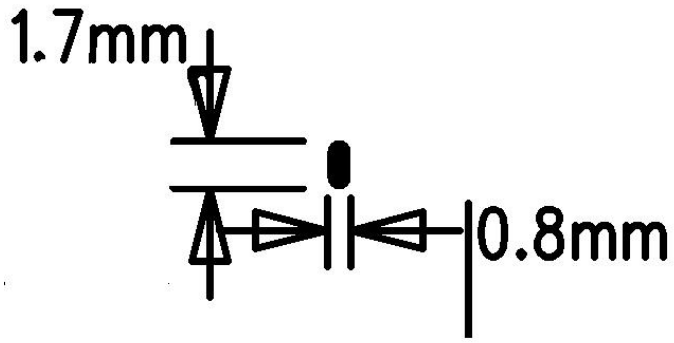


Fig.2 Pad diamension

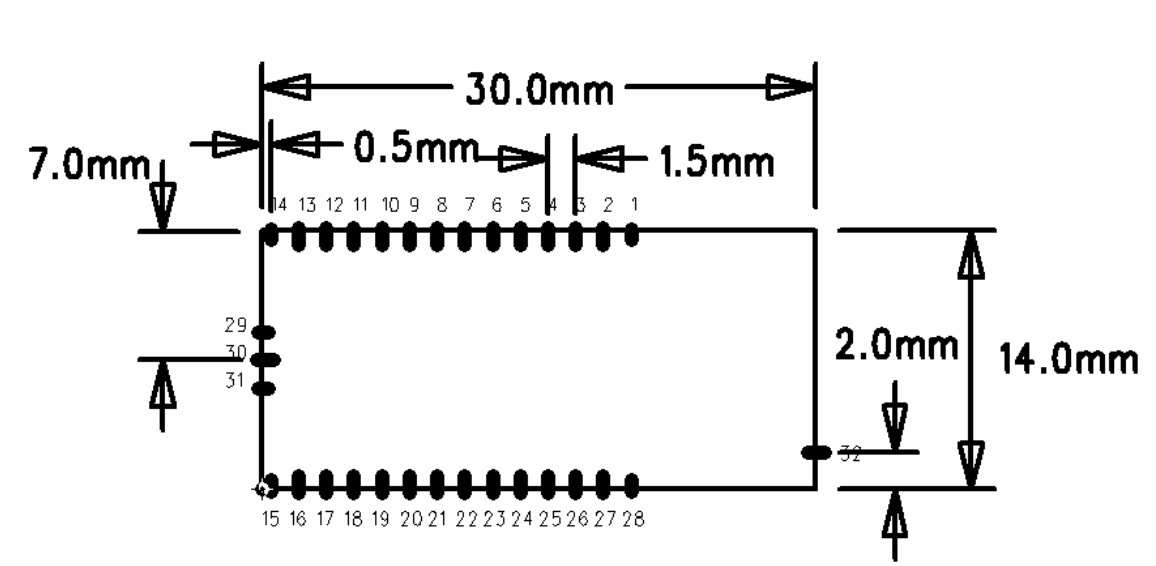


Fig.3 Module diamension

4. PCB layout consideration

As with any RF devices, the AUBTM-20 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized.

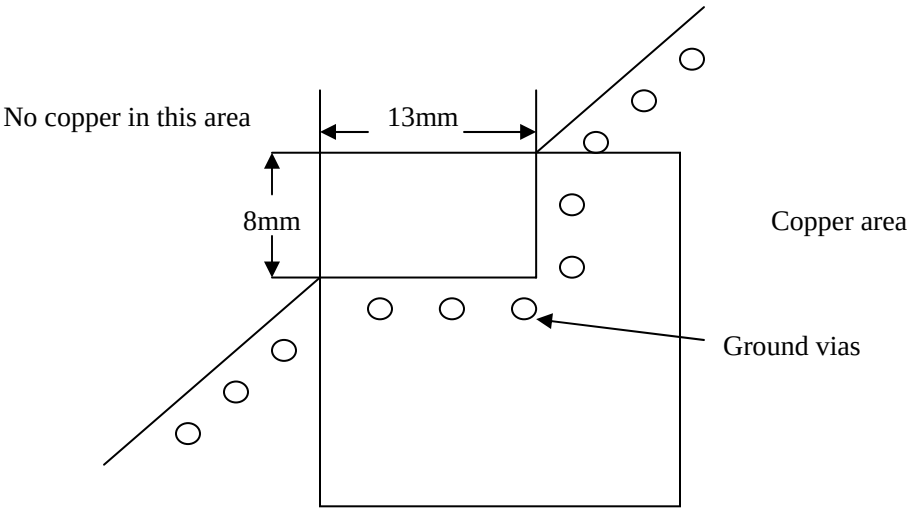


Fig.4 Copper area

Figures above illustrates how PCB design around the antenna of AUBTM-20 should be made. The most important thing is that there is no copper (ground plane or traces) underneath or in the close proximity of the antenna.

It's also very important to have grounding vias all the way in the border between ground plane and free space, as illustrated with black and gray dots in figures above. This prevents the RF signal for reflecting back to the PCB and signal lines over there.

Try to avoid any metal material near the antenna and keep at least 5mm away if it is inevitable. A solid ground should be provide for AUBTM-20 and the copper area should be at least 20x15mm to maintain the best RF performance.

5. Pin Configuration:

Pin Number	Pin name	I/O	
1	GND	GND	Ground
2	3V3	VDD	Power supply connection
3	PIO2	I/O	Programmable I/O lines
4	PIO3	I/O	Programmable I/O lines
5	NRTS	O	UART RTS (internal pull-up, active low)
6	RXD	I	UART RX (internal pull down)
7	PCMO	O	Synchronous 8 kbps data out (internal Pull down)
8	USB_D+	A	USB data plus (Internal 22 ohm serial resistor)
9	USB_D-	A	USB data minus (Internal 22 ohm serial resistor)
10	NCTS	I	UART CTS (internal pull down, active low)
11	PCMI	I	Synchronous 8 kbps data in (internal pull-down)
12	PCMC	I/O	Synchronous data clock (internal pull-down)
13	PCMS	I/O	Synchronous data strobe (internal pull-down)
14	GND	GND	Ground
15	GND	GND	Ground
16	3V3	VDD	Power supply connection
17	RES	I	Reset input (active low)
18	PIO6	I/O	Programmable I/O lines
19	PIO7	I/O	Programmable I/O lines
20	PIO4	I/O	Programmable I/O lines
21	NCSB	I	Chip selection for SPI (internal pull up, active low)
22	SCLK	I/O	SPI Clock (internal pull down)
23	MISO	O	SPI data output (pull down)
24	MOSI	I	SPI data input (pull down)
25	PIO5	I/O	Programmable I/O lines
26	TXD	O	UART TX (internal pull up)
27	NC	-	NC, not used
28	GND	GND	Ground
29	AIO0	I/O	
30	AIO1	I/O	
31	AIO2	I/O	
32	RF	RF	RF-transceiver antenna (when chip antenna not in use!)

List 1. pin assignment

6. Device Terminal Descriptions

6.1 UART

AUBTM-20 UART provides the main interface to exchange data with other host system using the RS232 protocol. An external commands set is provided for the host system to control and configure AUBTM-20.

Four signals are provide for UART function. TXD and RXD transmit data between AUBTM-20 and the host. NRTS and NCTS provides the RS232 hardware flow control mechanism. All UART pins are CMOS logic with signal levels of 0V to VDD.

UART is initially configured to work at 9600 bps baudrate, 8-bit, no parity and 1 stop bit. The host could reconfigure the UART by issuing command.
Possible UART setting is as the following:

6.2 PCM

Pulse Code Modulation (PCM) is a standard method used to digitize audio (particularly voice) patterns for transmission over digital communication channels. Through its PCM interface, AUBTM-20 has hardware support for continual transmission and reception of PCM data, thus reducing processor overhead for wireless headset applications. AUBTM-20 offers a bi directional digital audio interface that routes directly into the baseband layer of the on chip firmware. It does not pass through the HCI protocol layer.

Hardware on AUBTM-20 allows the data to be sent to and received from a SCO connection.

Up to three SCO connections can be supported by the PCM interface at any one time1.

AUBTM-20 can operate as the PCM interface Master generating an output clock of 128, 256 or 512kHz. When configured as PCM interface slave it can operate with an input clock up to 2048kHz. AUBTM-20 is compatible with a variety of clock formats, including Long Frame Sync, Short Frame Sync and GCI timing environments.

It supports 13 or 16-bit linear, 8-bit μ-law or A-law companded sample formats at 8ksamples/s and can receive and transmit on any selection of three of the first four slots following PCM_SYNC.

AUBTM-20 interfaces directly to PCM audio devices including the following:

• Qualcomm MSM 3000 series and MSM 5000 series CDMA baseband devices

- OKI MSM7705 four channel A-law and μ-law CODEC
- Motorola MC145481 8-bit A-law and μ-law CODEC
- Motorola MC145483 13-bit linear CODEC
- STW 5093 and 5094 14-bit linear CODECs

AUTBM-20 is also compatible with the Motorola SSI™ interface

6.3 GPIO

AUBTM-20 has 6 GPIO pin which could be used as digital signal input/output. Some of them has multiple functions. The signal level on these pins are 0V to VDD.

6.3.1 PIO2/SPP status indicator

When there is no SPP connection established, PIO2 will toggle its signal level every 0.1s. This could be used to drive a LED as the status indicator.

6.3.2 PIO3/SPP disconnect

A low to high transition on PIO3 will disconnect all the active SPP connection. A at least 5 ms of pulse for this signal is recommended.

6.3.3 PIO4

This pin has no multiple function.

6.3.4 PIO5/SPP Master/Slave Selection

PIO5 is monitored when the module is powered up. A high signal on this pin will make the module to enter SPP master mode, while a low signal on this pin will make the module to enter SPP slave mode.

6.3.5 PIO6/SCL PIO7/SDA

PIO6/PIO7 form a slow speed I2C interface which could be used to access LCD, Keyboard scanner or EEPROM. This I2C could only act a master and require pull-up

resisters as illustrated in Fig.
PIO6/PIO7 could also be used as general IO pin if I2C function is not implemented.

6.4 AIO

AUBTM-20 has three general purpose analog input/output pins. Each of them could be configured as both as 8-bit DAC or ADC. The host could use commands to read the value on the pin when it is an ADC or set its signal level when it is a DAC. The signal level of these pins are from 0V to VDD.

6.5 USB

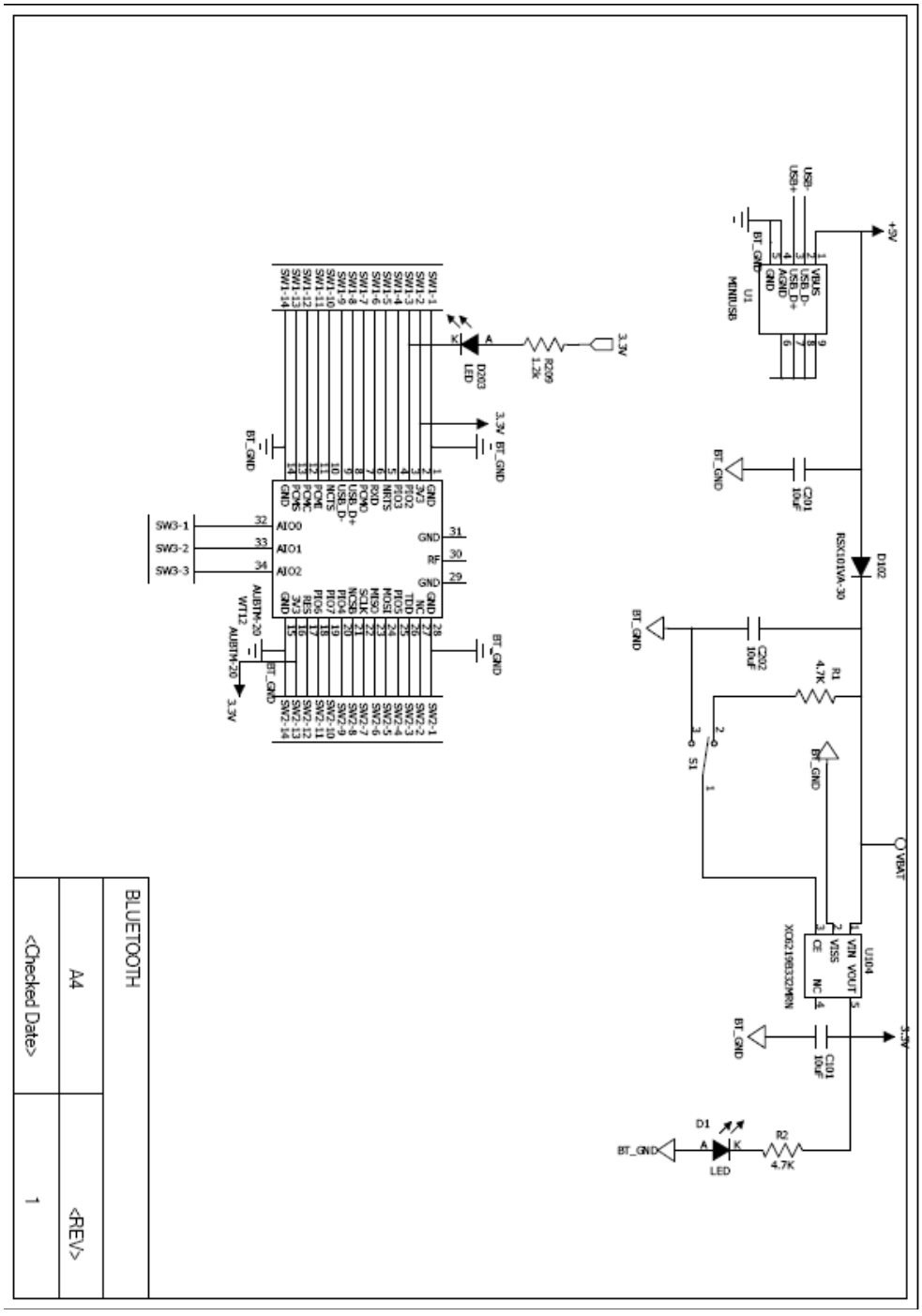
AUBTM-20 contains a full-speed (12M bps) USB interface which is capable to drive a USB cable directly without using a external USB transceiver. Note that AUBTM-20 could only work as a slave USB device.

The USB data lines emerge as pins USB_D+ and USB_D-. These terminals are connected to the internal USB I/O buffers of the AUBTM-20 and therefore have low output impedance. To match the connection to the characteristic impedance of the USB cable, resistors are included with USB_DP / USB_DN and the cable.

6.6 SPI

The synchronous serial port interface (SPI) for interfacing with other digital devices. The SPI port can be used for system debugging. It can also be used for programming the Flash memory. SPI interface is connected using the MOSI, MISO, CSB and CLK pins.

7. Application Schmatics



8. Electrical specification:

Radio Characteristics	Min	Typ	Max	Unit
Output Power	-6	2.5	4	dBm
Power control range	-	35	-	dB
Power control step	-	0.5	-	dB
Operation Current		70	110	mA
Sensitivity		-80	-70	dBm
Supply Voltage(VDD)	2.7	3.3	3.7	V

Digital Terminal Input voltage	Min	Typ	Max	Unit
VIL input logic level low (VDD=3.3V)	-0.4		+0.8	V
VIH input logic level high	0.7VDD		VDD+0.4	V
Digital Terminal Output voltage				
VOL output logic level low (VDD=3.3V) (lo = 3.0mA)			0.2	V
VOL output logic level high (VDD=3.3V) (lo = -3.0mA)	VDD-0.2			V

Input and Tri-state Current with:	Min	Typ	Max	Unit
Strong pull-up	-100	-40	-10	µA
Strong pull-down	+10	+40	+100	µA
Weak pull-up	-5.0	-1.0	-0.2	µA
Weak pull-down	+0.2	+1.0	+5.0	µA
I/O pad leakage current	-1	0	+1	µA
CI Input Capacitance	1.0	-	5.0	pF

USB Terminals Characteristics	Min	Typ	Max	Unit
VDD_USB for correct USB operation	3.1		3.6	V
Input threshold				
VIL input logic level low	-	-	0.3VDD	V
VIH input logic level high	0.7VDD	-	-	V
Input leakage current				
VSS < VIN < VDD	-1	1	5	µA
CI Input capacitance	2.5	-	10.0	pF
Output Voltage levels to correctly terminated USB Cable				
VOL output logic level low	0.0	-	0.2	V

VOH output logic level high	2.8	-	VDD	V

Auxiliary ADC		**Min**	**Typ**	**Max**	**Unit**
Resolution		-	-	8	Bits
Input voltage range (LSB size = VDD/255)		0	-	VDD	V
Accuracy(Guaranteed monotonic)	INL	-1	-	1	LSB
	DNL	0	-	1	LSB
Offset		-1	-	1	LSB
Gain Error		-0.8	-	0.8	%
Input Bandwidth		-	100	-	kHz
Conversion time		-	2.5	-	μs
Sample rate(2)		-	-	700	Samples/s

9. SOLDERING

9.1 Manual Soldering

TBA

9.2 Reflow soldering

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder re-flow. There are four zones:

1. Preheat Zone - This zone raises the temperature at a controlled rate, typically 1-2.5°C/s.

2. Equilibrium Zone - This zone brings the board to a uniform temperature and also activates the flux. The duration in this zone (typically 2-3 minutes) will need to be adjusted to optimize the out gassing of the flux.

3. Reflow Zone - The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint.

4. Cooling Zone - The cooling rate should be fast, to keep the solder grains small which will give a longer lasting joint. Typical rates will be 2-5°C/s.

5. Solder Re-Flow Profile for Devices with Lead-Free Solder Balls

Composition of the solder ball: Sn 95.5%, Ag 4.0%, Cu 0.5%

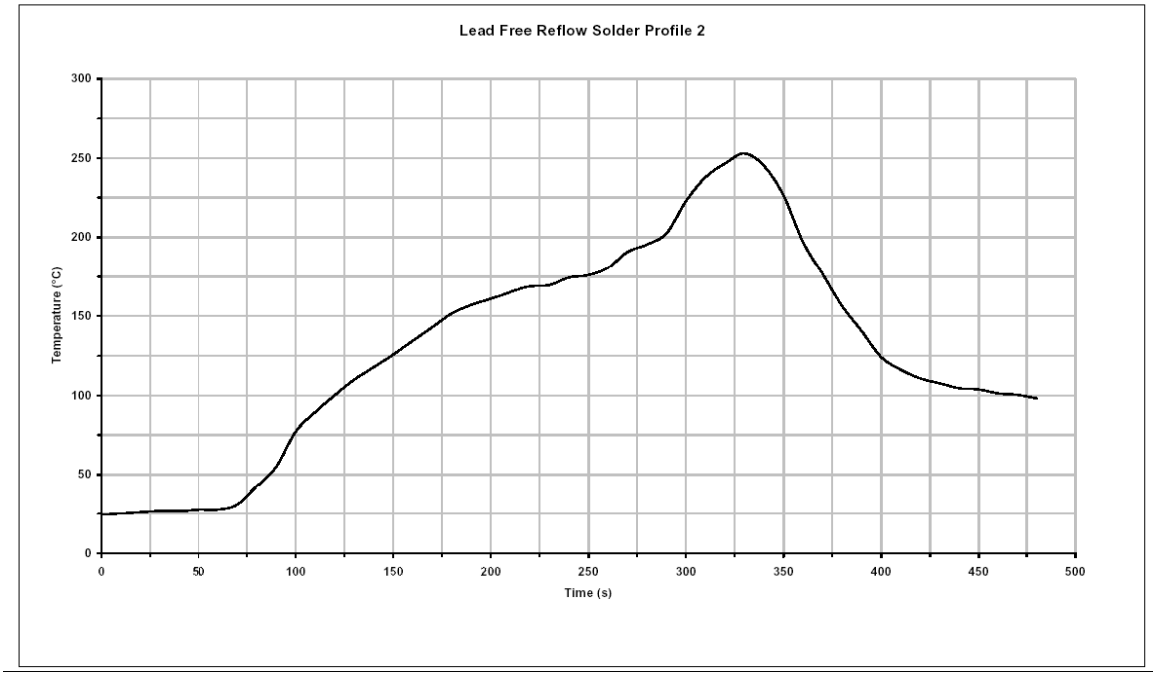


Figure 34: Reflow solder profile

Key features of the profile:

- Initial Ramp = 1-2.5°C/sec to 175°C±25°C equilibrium
- Equilibrium time = 60 to 180 seconds
- Ramp to Maximum temperature (250°C) = 3°C/sec max.
- Time above liquidus temperature (217°C): 45-90 seconds
- Device absolute maximum reflow temperature: 260°C

Devices will withstand the specified profile. Lead-free devices will withstand up to three reflows to a maximum temperature of 260°C.

Revision History

DATE	VERSION	DESCRIPTION
Jun 20, 2006	a	Preliminary publication
Aug 16, 2007	b	Restructure of the document

NOTES

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