Electronics Club

Verilog Lecture Series
IIT KANPUR

Assign Statement

- An assign statement is used for modeling only combinational logic
- it is executed continuously without any sensitivity list (like always @(a or b))

Test Bench

- All inputs to be declared as reg and outputs as wire
- It has no port list

Delays

- #t gives delay of time t
- Frequency Generator

Examples

Hello in german

Counter

Adder 1 bit

Adder 4 bit

Instantiation